POWERLINK
+ Open Source IP-Core
=> FPGA

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Initial Questions

- **POWERLINK:**
  What is the working principle?

- **Open Source IP-Core:**
  What is provided?

- **FPGA:**
  What is an FPGA and why do we need one?
POWERLINK?

● Who?
Sensors, control, actuators.

● What?
Process data,
like state of digital inputs and outputs, analog values, temperatures, speed, …

● How?
Deterministic transmission of process data over Ethernet.
What is POWERLINK?

- Industrial Ethernet Fieldbus Protocol (see [1])
- Based on IEEE 802.3u Fast Ethernet
- CANopen over Ethernet
- Real-time capable via slot communication
- Master-Slave Protocol
  - Master = Managing Node (MN)
  - Slave = Controlled Node (CN)
- Hot plugging
- Direct cross-traffic
What is openPOWERLINK?

- Open Source implementation of POWERLINK
- Development done by SYS TEC electronic GmbH
- Currently supported target platforms:
  - Linux
  - Windows
  - bare-metal (OS-less)
- License: BSD
- Pure software-based solution on standard Ethernet controllers, but hardware-acceleration possible
How does POWERLINK work?

Slot Communication Network Management

Diagram: CycleTime with slots for SoC, PReq CN1, PReq CN2, PReq CN3, PReq CNn, SoA, PRes CN1, PRes CN2, PRes CN3, PRes CNn, Async Data, Isochronous Phase, Asynchronous Phase, MN, CN.
SoC Frame

**SoC**: Start of Cycle synchronization event
PReq Frame

**PReq**: Poll Request from MN for specific CN contains PDO payload
**PRes Frame**

**PRes**: Poll Response from CN / MN contains PDO payload and current NMT state
**SoA Frame**

**SoA**: Start of Asynchronous assigns asynchronous phase to specific node
ASnd Frame

**ASnd**: Asynchronous Send
NMT commands, SDO, IdentResponse, StatusResponse

TCP/IP
Crucial Point on CN

Latency between PReq and PRes
Solution Idea

- Ethernet controller with auto-response feature
- PRes frame is sent on reception of PReq by HW
- No intervention of SW necessary
- Deterministic response time (inter frame gap = 96 bit)

- TI AM335x with Programmable Real-Time Unit and Industrial Communication Subsystem
- Hilscher netX (integrated proprietary communication controller)
- VHDL implementation as open source available
FPGA

- Field Programmable Gate Array
  = coll. “programmable hardware”
- Vendors: Altera, Lattice, Xilinx, …
- Programming languages: VHDL and Verilog
- Higher level design tools for entire System-on-Chips with Soft CPUs and peripherals:
  e.g. Altera SOPC Builder / Qsys with NIOS II, Xilinx ISE with Microblaze
openMAC

- VHDL source under BSD license
- 100 Mbit/s Ethernet controller with RMII
- 50 MHz clock design
- 16 Rx filters with 31 bytes value and mask
- 16 Rx descriptors
- 16 Tx descriptors
- Time stamping of Rx frames with 20 ns clock
FPGA Design

Altera Cyclone III FPGA

- POWERLINK IP-Core
- NIOS II
- RAM
- GPIO

PHY

Ethernet POWERLINK
Advantages of FPGAs

- Determinism by clocked HW design
- Parallel processing
- Simple PCB with few components
- Flexibility: programmable hardware
References


Any questions about FPGAs, POWERLINK or openPOWERLINK?

Thanks for your attention!
Topology

Possible Topologies:
• Star
• Line (daisy chain)
• Tree
• Mixed

Connectors:
• RJ45
• M12

Equipment:
• Hubs
• Switches